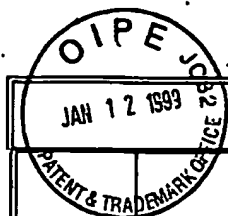


FORM PTO-1449 (REV. 7.80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. ST No.: 97-C-108 119932-1012		SERIAL NO. 09/360,824	
LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Tsiu Chiu Chan, et al.		RECEIVED MAR 26 1999 GROUP 2100	
				FILING DATE 9/25/98		RECEIVED JAN 20 1999 GROUP 2100	
U. S. PATENT DOCUMENTS							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)	
Tb	4,774,632	9/27/88	Hybrid Integrated Circuit Chip Package	361	386	7/6/87	
Tb	5,019,673	5/28/91	Flip-Chip Package for Integrated Circuits	174	52.2	8/22/90	
Tb	5,093,708	3/3/92	Multilayer Integrated Circuit	357	68	8/20/90	
Tb	5,107,586	4/28/92	Method for Interconnecting a Stack of Integrated Circuits at a Very High Density	29	830	3/15/91	
Tb	5,122,691	6/16/92	Integrated Backplane Interconnection Architecture	307	475	11/21/90	
Tb	5,217,914	6/8/93	Method for Making Semiconductor Integration Circuit with Stacked Capacitor Cells	437	47	4/10/91	
Tb	5,265,045	11/23/93	Semiconductor Integrated Circuit Device with Built-In Memory Circuit	365	63	11/15/91	
Tb	5,346,857	9/13/94	Method for Forming a Flip-Chip Bond from a Gold-Tin Eutectic	437	183	9/28/92	
Tb	5,377,077	12/27/94	Ultra High Density Integrated Circuit Packages Method and Apparatus	361	704	12/17/93	
Tb	5,399,898	3/21/95	Multi-Chip Semiconductor Arrangements Using Flip Chip Dies	257	499	11/12/92	
Tb	5,454,160	10/3/95	Apparatus and Method for Stacking Integrated Circuit Devices	29	840	12/3/93	
To	5,650,977	7/22/97	Integrated Circuit Memory Device Including Banks of Memory Cells and Related Methods	368	230.03	4/25/96	
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Tsiu Chiu Chan 4/26/05



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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION (Abstract)	
						YES	NO
TD	148,857 -	1981	Japan	25	06	X	
TD	137,655 -	1981	Japan	25	06	X	
TD	224,154 -	1984	Japan	23	48	X	
TD	155,162 -	1984	Japan	25	06	RECEIVED JAN 7 11 1999	
TD	127,856 -	1984	Japan	25	06		
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TD	5,540 -	1990	Japan	21	60	X	
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TD	276,751 -	1991	Japan	25	065	X	
TD	276,750 -	1991	Japan	25	065	X	

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TD	266,454 /	1991	Japan	23	04	x
	231,450 /	1991	Japan	25	065	x
	173,170 /	1991	Japan	27	00	x
	169,062 /	1991	Japan	25	065	x
	69,150 /	1991	Japan	25	065	x
	44,955 /	1991	Japan	23	50	x
	276,750 *	1991	Japan	25	065	x
TD	3,263 /	1991	Japan	25	10	RECEIVED
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	274,356 /	1992	Japan	25	065	x
	256,352 /	1992	Japan	25	04	x
	180,257 /	1992	Japan	25	065	x
	158,565 /	1992	Japan	25	065	x
	116,861 /	1992	Japan	25	16	x
	76,946 /	1992	Japan	27	00	x
	62,961 /	1992	Japan	25	04	RECEIVED
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TD	48,768 /	1992	Japan	25	065	x
TD	160,325 /	1993	Japan	23	50	Group 2700
	129,517 /	1993	Japan	25	065	x
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	90,486 /	1993	Japan	25	065	x
	55,451 /	1993	Japan	25	065	x
	48,001 /	1993	Japan	25	065	x
	13,667 /	1993	Japan	25	16	x
	13,663 /	1993	Japan	25	065	x
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	259,378 /	1993	Japan	27	00	x
	243,482 /	1993	Japan	25	065	x
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TD	183,010 /	1993	Japan	21	60	x
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TD	112,401	1994	Japan	25	065	X
TD	21,328	1994	Japan	25	065	X
TD	5,778	1994	Japan	25	065	X
TD	350,025	1994	Japan	25	10	X
TD	302,762	1994	Japan	25	065	X
TD	241,889	1994	Japan	1	02	X
TD	188,362	1994	Japan	25	065	X
TD	188,280	1994	Japan	21	60	X
TD	150,031	1994	Japan	15	78	X
TD	132,474	1994	Japan	25	065	X
TD	211,758	1995	Japan	21	66	X
TD	169,909	1995	Japan	25	10	X
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TD	307,437	1995	Japan	25	065	X
TD	221,135	1995	Japan	21	60	X
TD	264,712	1996	Japan	25	065	X
TD	167,703	1996	Japan	27	108	X
TD	125,112	1996	Japan	25	065	X
TD	152,979	1997	Japan	11	22	X
TD	55,390	1997	Japan	21	50	X
TD	17,945	1997	Japan	25	065	X
TD	17,913	1997	Japan	23	28	X

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Pentium® Pro processor a tour of the Microarchitecture, Website
<http://www.intel.com/procs/ppro/info/p6white/index.htm>

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.